IN THE CLAIMS

Please amend the claims as follows:

1. (original) A circuit arrangement (100) for controlling at least one transistor
(10, 12, 14, ... ,18), especially for controlling the resistance value of at least one MOS transistor with vanishing DC modulation, characterized in that in addition to at least one first reference element (10, 20, 70), which comprises at least one first reference transistor (10) with a first offset from the operating point, at least a second reference element (12, 30, 40, 72, 74, 76) is provided, which comprises at least a second reference transistor (12) with a second offset from the operating point equal in value but opposed in sign to the first offset, wherein in particular an arithmetic mean can be taken of the first offset and the second offset for approximating and reaching an optimum operating point.

2. (original) A circuit arrangement as claimed in claim 1, characterized by

- at least an external resistor (78) by means of which a reference current (Iref) produces a voltage (Ur) on the basis of a reference voltage (Uref) ,

- the first reference transistor (10), by means of which a first current (11) corresponding in value and in sign to the reference current (Iref) produces a first voltage (U1),
- at least a first buffer element (20) connected next in line to the drain connection (10d) of the first reference transistor (10) or to the source connection (10s) of the first reference transistor (10),
- at least a first resistor (70) connected next in line to the output connection (20o) of the first buffer element (20),

at least a second reference transistor (12) by means of which a second current (I2) equal but opposed to the first current (I1) produces a second voltage (U2),

- at least a second buffer element (30) connected to the drain connection (12d) of the second reference transistor (12) or to the source connection (12s) of the second reference transistor (12),
- at least an operational amplifier (40), in particular an inverting amplifier with amplification factor -1,
  - whose first, negative input connection (40i1) is connected next in line to the output connection (30o) of the second buffer element (30) and
  - whose second, positive input connection (40i2) is charged with the reference voltage (Uref), wherein the

second voltage (U2) is capable of being inverted to an inverted second voltage (U2inv) with respect to the reference voltage (Uref),

- at least a second resistor (72) connected next in line to the output connection (40o) of the operational amplifier (40),
- at least a comparator element (50),
  - whose first, positive input connection (50i1) is connected next in line to the first resistor (70) and to the second resistor (72) in order to charge this first input connection (50i1) of the comparator element (50) with a mean voltage (Um) averaged over the first resistor (70) and the second resistor (72), and
  - whose second, negative input connection (50i2) is charged with the voltage (Ur) produced by means of the external resistor (78),
- at least a condenser element (60) connected next in line to the output connection (50o) of the comparator element (50), which can be charged and discharged by the comparator element (50) as a function of the result of a comparison between the mean voltage value (Um) and the voltage (Ur) produced by the external resistor (78), wherein the respective gates (10g, 12g, 14g, ..., 18g) of the first reference transistor (10), the second reference transistor (12) and of all further transistors to be controlled

(14, ..., 18), as applicable, can be fed with the voltage (Uc) of condenser element (60) serving as a control voltage, and/or wherein the optimum operating point corresponding to the control voltage (Uc) is reached, the moment the mean voltage value (Um) corresponds to the voltage (Ur) produced by the external resistor (78).

3. (original) A circuit arrangement as claimed in claim 2, characterized in that the source connection (10s) of the first reference transistor (10) or the drain connection (10d) of the first reference transistor (10) and

- the source connection (12s) of the second reference transistor (12) or the drain connection (12d) of the second reference transistor (12) are chargeable with the reference voltage (Uref).

4. (currently amended) A circuit arrangement as claimed in claim 2~~ or 3~~, characterized in that

- the first voltage (U1) is lower than the reference voltage (Uref) and/or

- the second voltage (U2) is higher than the reference voltage (Uref).

5. (currently amended) A circuit arrangement as claimed in ~~one of the claims 2 to 4~~claim 2, characterized in that,

- at least a third resistor (74) is connected between the output connection (30o) of the second buffer element (30) and the first, negative input connection (40i1) of the operational amplifier (40), and/or

- at least a fourth resistor (76) is connected parallel to the first, negative input connection (40i1) of the operational amplifier (40) and to the output connection (40o) of the operational amplifier (40).

6. (original) A method of controlling at least a transistor (10, 12, 14,…, 18), particularly of controlling the resistance value of at least one MOS transistor with vanishing DC modulation, characterized in that

- a first reference transistor (10) produces a positive voltage drop (U1), especially a positive DC voltage drop,

- a second reference transistor (12) produces a negative voltage drop (U2), especially a negative DC voltage drop,

- the negative voltage drop (U2) is inverted to an inverted voltage drop (U2inv)

- an arithmetic mean voltage value (Um) is formed from the positive voltage drop (U1) and the inverted voltage drop (U2inv)

and is compared with an externally caused voltage drop (Ur), in particular an externally caused DC voltage drop, and

- the first reference transistor (10), the second reference transistor (12) and any additional transistors (14,..., 18) to be controlled, as applicable, are regulated by means of a control voltage (Uc) formed by the comparison of the mean voltage value (Um) and the externally caused voltage drop (Ur).

claims 7-10 (canceled)